IN THE CLAIMS:

Please cancel claims 18-20, 27-29, 34 and 40-42 and amend the claims as follows:

1. (Currently Amended): A digital processing system comprising a pipelined architecture for decoding convolutional encoded data comprising:

circuit means for performing branch metrics calculations;

circuit means for performing path metrics calculations;

survivor storage for retaining survivor bits indicating a preferred path through a tree;

a pipeline register for receiving a word of survivor bits from said survivor storage; and

a trace-back circuit for selecting a tree path and for determining a next address in said survivor storage of a trace bit, [[; and]] the trace back circuit including means for compensating for a delay introduced by said pipeline register by adjusting the memory read address, wherein the survivor bits are stored across multiple memory words, each of the trace bits being used to address one of the multiple memory words.

2. (Original): The digital processing system of Claim 1 wherein said compensating means comprises storage of said survivor bits in a non-ordinal sequence.

3. (Original): The digital processing system of Claim 1 wherein said compensating means comprises storage of said survivor bits based on an optimized subsection of said tree.

4. (Original): The digital processing system of Claim 1 wherein said compensating means comprises storage of said survivor bits based on a final state distribution.

5. (Currently Amended): The digital processing system of Claim 1 wherein the selection of a survivor bit ~~for~~ includes addressing a word from said survivor storage for transfer to said pipeline register.

6. (Currently Amended): The digital processing system of Claim 1 wherein said pipeline comprises a single stage and said memory is organized into an even word and an odd word, the survivor bits for all even states being stored in an even addressed word and the survivor bits for all odd states being stored in an odd addressed word.

7. (Original): The digital processing system of Claim 6 wherein said even word corresponds to the following states: 0, 32, 16, 48, 8, 40, 24, 56, 4, 36, 20, 52, 12, 44, 28, 60, 2, 34, 18, 50, 10, 42, 26, 58, 6, 38, 22, 54, 14, 46, 30 and 62.

8. (Original): The digital processing system of Claim 6 wherein said odd word corresponds to the following states: 1, 33, 17, 49, 9, 41, 25, 57, 5, 37, 21, 53, 13, 45, 29, 61, 3, 35, 19, 51, 11, 43, 27, 59, 7, 39, 23, 55, 15, 47, 31, and 63.

9. (Original): The digital processing system of Claim 1 wherein said pipeline comprises a single stage and said memory is organized into two 32 bit memory words.

10. (Original): The digital processing system of Claim 1 wherein said pipeline comprises a single stage and said memory is organized into a first word for storing the first 16 bits and bits 32-47 and a second word for storing bits 16-31 and bits 48-63.

11. (Original): A method for obtaining the maximum likelihood sequence estimate of bits in a data stream from a convolutionally encoded received data stream comprising the steps of:

Performing the following steps for each received bit in said encoded received data stream:

a. Determining a trace-back length;

b. Obtaining a Trellis diagram of the convolutional encoder that generated said encoded received data stream;

~~c. Obtaining a Trellis diagram of the convolutional encoder that generated said encoded received data stream;~~

~~d.~~ c. For each bit in said received data stream, perform a plurality of forward butterfly computations to determine survivor path bits;

~~e.~~ d. For each butterfly computation, storing the resulting survivor path bits for each state in a trace-back memory;

~~f.~~ e. For each butterfly computation, updating path metrics for a pair of states and generating a pair of survivor bits; and

~~g.~~ f. Repeating steps ~~a-[[g]]~~ f for each bit until all bits in the encoded received data stream have been recorded;

Selecting a trace-back window;

Sequentially decrementing by a 2 32-bit word steps to access a trace-back memory;

Extracting a trace bit to perform a look-ahead function to determine a computed address of a future survivor word;

Determining whether said future survivor word is an even or odd state;

Determining a decoded bit from said computed address; and

Outputting ~~an unencoded~~ decoded data stream corresponding to said encoded received data stream.

12. (Original): The method of Claim 11 wherein the information stored in said trace-back memory is partitioned.

13. (Original): The method of Claim 12 wherein the information stored in said trace-back memory is partitioned into an even partition and an odd partition.

14. (Original): The method of Claim 13 wherein said memory partitions correspond to a code tree.

15. (Original): The method of Claim 13 wherein the constraint length (k) of said encoder is an odd integer.

16. (Original): The method of Claim 12 wherein the parameters of said encoder are: rate (r) where r = ½; constraint length (k) where k – 7; and generator polynominals $g_0 = 133|_8$ and $g_1 = 171|_8$.

17. (Original): The method of Claim 12 wherein the said encoders has a rate (r) where r = ½ and a constraint length (k), where k = 9.

18 – 20 (Cancelled)

21. (Currently Amended): A method for implementing a Viterbi decoder including a pipelined architecture comprising the steps of:

Receiving convolutionally encoded data;

Generating a tree for said encoded data;

Calculating branch metrics;

Calculating path metrics to determine survivor bits indicating a preferred path through [[a]] the tree;

Retaining said survivor bits in a survivor storage comprising a pipeline register ~~memory~~;

Selectively accessing words in said ~~memory~~ survivor storage using a look-ahead pipeline in the pipelined architecture;

~~a trace-back circuit for~~ selecting a tree path for determining a next address in said survivor storage of a trace bit based on one or more of the survivor bits; and

~~means for~~ compensating for ~~the~~ a delay introduced by said pipeline register by adjusting the memory read address wherein the survivor bits are stored across multiple memory words, each of the trace bits being used to address one of the multiple memory words and access the addressed memory word.

22. (Original): The method of Claim 21 wherein the information stored in said trace-back memory is partitioned.

23. (Original): The method of Claim 21 wherein the information stored in said trace-back memory is portioned into an even partition and an odd partition.

24. (Original): The method of Claim 23 wherein said memory partitions correspond to a tree.

25. (Original): The method of Claim 22 wherein the parameters of said encoder are: rate (r) where r = ½; constraint length (k) where k – 7; and generator polynominals $g_0 = 133|_8$ and $g_1 = 171|_8$.

26. (Original): The method of Claim 22 wherein the said encoders has a rate (r) where r – ½ and a constraint length (k) where k = 9.

27 – 29 (Cancelled)

30. (Currently Amended): A method for implementing a Viterbi decoder, ~~having~~ including a pipeline register, that maintains data throughput and integrity by organizing a memory for storing survivor bits to account for pipeline delay where said organization is based upon the properties of the code tree comprising the steps of:

~~Organizing a memory for storing survivor bits to account for pipeline delay where said organization is based upon the properties of the code tree;~~

Receiving convolutionally encoded data;

Decoding said received convolutionally encoded data including the steps of;

[[and]]

generating a tree for said encoded data;

calculating branch metrics;

calculating path metrics to determine survivor bits indicating a preferred path through the tree;

retaining said survivor bits in a survivor storage comprising a pipeline register;

selectively accessing words in said survivor storage using a look-ahead pipeline in the pipelined architecture;

selecting a tree path for determining a next address in said survivor storage of a trace bit based on one or more of the survivor bits;

compensating for a delay introduced by said pipeline register by adjusting the memory read address, wherein the survivor bits are stored across multiple memory words, each of the trace bits being used to address one of the multiple memory words and access the addressed memory word; and

~~Outputting~~ outputting data corresponding to said received convolutionally encoded data.

31. (Original): The method of Claim 30 wherein said memory is organized so that the storage of survivor bits is in a non-ordinal sequence.

32. (Original): The method of Claim 30 wherein said memory is organized so that the storage of said survivor bits is based on an optimized subsection of a code tree.

33. (Original): The method of Claim 32 wherein said code tree is defined by the parameters of said encoder.

34. (Cancelled)

35. (Currently Amended): The method of Claim 30 wherein said memory is organized into an even word and an odd word, the survivor bits for all even states being stored in an even addressed word and the survivor bits for all odd states being stored in an odd addressed word.

36. (Original): The method of Claim 30 wherein said even word corresponds to the following states: 0, 32, 16, 48, 8, 40, 24, 56, 4, 36, 20, 52, 12, 44, 28, 60, 2, 34, 18, 50, 10, 42, 26, 58, 6, 38, 22, 54, 14, 46, 30 and 62.

37. (Original): The method of Claim 30 wherein said odd word corresponds to the following states: 1, 33, 17, 49, 9, 41, 25, 57, 5, 37, 21, 53, 13, 45, 29, 61, 3, 35, 19, 51, 11, 43, 27, 59, 7, 39, 23, 55, 15, 47, 31 and 63.

38. (Original): The method of Claim 37 wherein said pipeline comprises a single stage and said memory is organized into two 32-bit memory words.

39. (Original): The method of Claim 30 wherein said pipeline comprises a single stage and said memory is organized into a first word for storing the first 16 bits and bits 32-47 and a second word for string bits 16-31 and bits 48-63.

40 – 42 (Cancelled)

43. (New): The digital processing system of claim 1 wherein the survivor bits represents a portion of the path in the survivor path but does not represent a decoded bit of the data.

44. (New):The digital processing system of claim 1 wherein the trace back circuit extracts trace bits from the word of survivor bits, each of the trace bits determining the address computation of the survivor word for a later cycle, and whether the address to be computed if cycles later is an even or odd state.